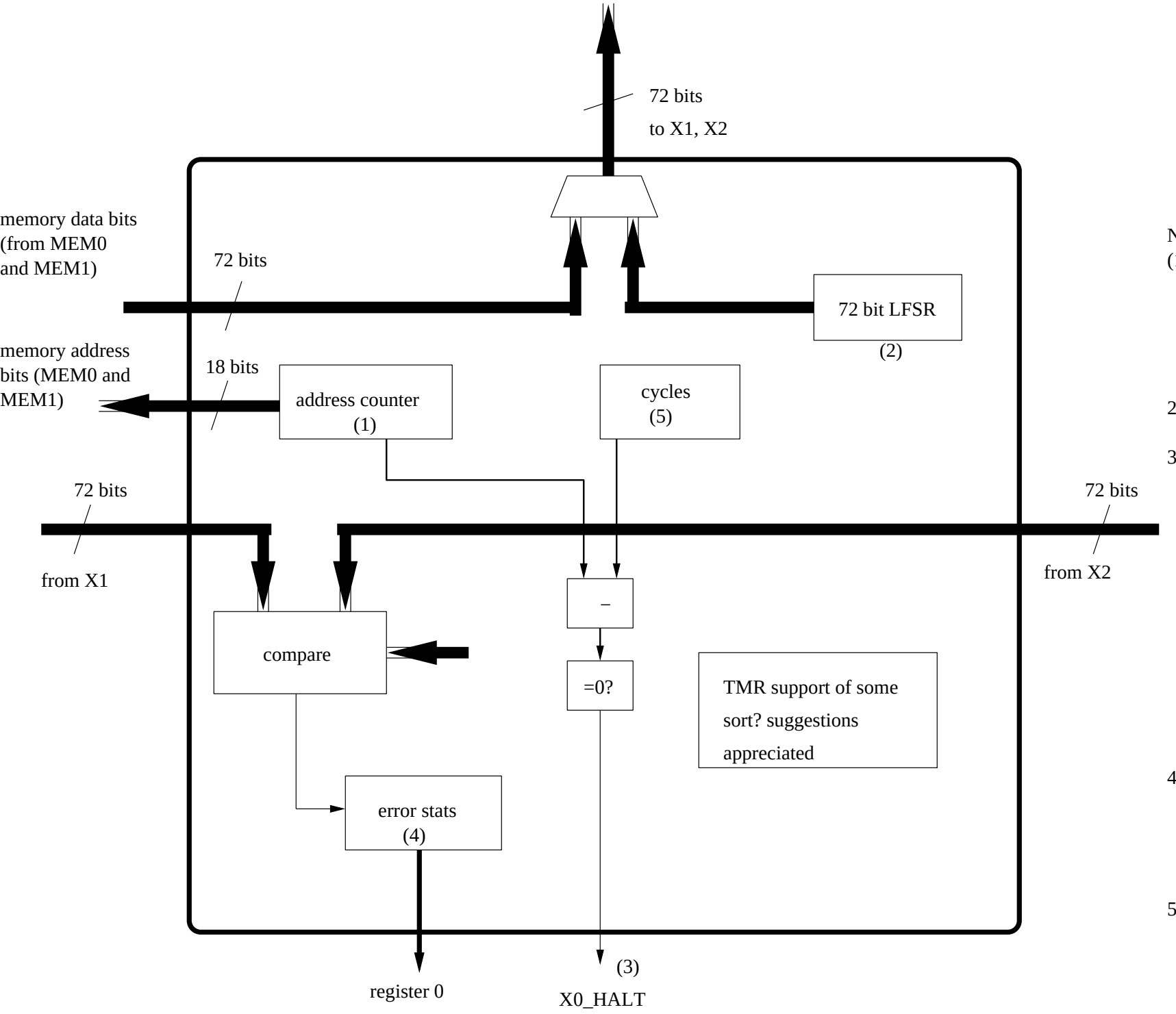
Proposed X0 Architecture for SEU Studies



Notes

(1) incorporate into the reset() call the reset for this counter and ensure that X0 is clocked enough times to gaurantee the presence of data on the memory data line (memory latency

2) should this be reset every time we perform a reset?

3) this could be an interrupt/stop clock signal. From the time the stop clock signal is asserted, the PEs will see 3 more rising edges. Also, memory latency has a play here. If we wish to stop after the circuit has seen the data at location 10, we should assert this signal on cycle (10+1−3−memcycles), where memcycles=4 if in pipelined mode, =3 if in flow_through mode
we can check this by testing X0_MEM_MODE, which is 1 if pipelined, 0 if flow_through

4)keeps track of:

- number of errors observed
- cycles since the first observed error
- cycles since the most recently observed error

5) the user can set the number of cycles desired to run until the clock stops. This can guarantee that the desired number of test vector inputs will be seen by X1 and X2 designs